IFW
AF2822

Docket No.: WMP-IFT-699

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: September 24, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/073,847 Confirmation No.: 6635
Inventor	:	Matthias Stecher et al.
Filed	:	February 11, 2002
Title	:	SOI Component
TC/A.U.	:	2822
Examiner	:	Mark V. Prenty
Customer No.	**:**	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated June 1, 2004, finally rejecting claims 1, 2, 5, 6, 8, 10, 11 and 13.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

09/27/2004 AADOF01 00000061 10073847
01 FC:1402 330.00 OP

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1, 2, 5, 6, 8, 10, 11 and 13 are rejected and are under appeal. Claim 7 was cancelled in an amendment filed June 10, 2003. Claims 3, 4, 9, 12 and 14 are objected to by the Examiner.

Status of Amendments:

No claims were amended after the final Office action. *A Notice of Appeal* was filed on August 5, 2004.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to a semiconductor component that includes a semiconductor substrate, an insulation layer located on the

semiconductor substrate, a semiconductor layer configured on the insulation layer, a first doped terminal zone and a second doped terminal zone that are formed in the insulation layer, and a drift zone that is formed in the insulation layer and between the first doped terminal zone and the second doped terminal zone.

Appellants explained on page 11 of the specification, line 22, that, in all of the figures, unless otherwise specified, identical reference symbols designate identical parts and sections with the same meaning.

Appellants outlined on page 12 of the specification, line 1, that, referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a cross sectional view of a semiconductor component that is designed as a diode. The component has a semiconductor substrate 10 with an insulation layer 20 formed on the semiconductor substrate 10. The semiconductor substrate 10 is preferably composed of silicon, and the insulation layer 20 of silicon oxide or silicon nitride. A semiconductor layer 12 is arranged on the insulation layer 20. A first terminal zone 30 and a second terminal zone 40 are formed in the semiconductor layer 12. A drift zone 32 is formed in the semiconductor layer 12 and between the first and second terminal zones 30, 40. The

first terminal zone 30 directly adjoins the semiconductor substrate 10, and in the exemplary embodiment, extends through the insulation layer 20 right into the semiconductor substrate 10.

Appellants further outlined on page 12 of the specification, line 18, that the semiconductor substrate 10 and the first terminal zone 30, which directly adjoins the semiconductor substrate 10, are doped complementary. In the exemplary embodiment, the substrate 10 is p-doped and the first terminal zone 30 is n-doped. The doping type of the semiconductor substrate 10 and the doping type of the adjoining first terminal zone 30 are chosen, taking account of the potentials that are expected at the substrate 10 and the first terminal zone 30, such that the semiconductor junction between the first terminal zone 30 and the substrate 10 is always reverse-biased or free of voltage. If the substrate 10 is, as usual, at the lowest potential occurring in the circuit, for example ground GND, then the potential at the first terminal zone 30 can correspond to that of the substrate 10 and the semiconductor junction is then free of voltage, or the potential at the first terminal zone 30 can be greater than the potential of the substrate 10 and the semiconductor junction is then reverse-biased.

Appellants described on page 13 of the specification, line 10, that, if the substrate 10 is always at the highest potential in the circuit, then, in contrast to the illustration in the exemplary embodiment, the first terminal zone 30 is p-doped and the substrate 10 is n-doped.

It is further described on page 13 of the specification, line 15, that the first n-doped terminal zone 30 forms the cathode K of the component which is designed as a diode and illustrated in Fig. 1, and the p-doped second terminal zone 40 forms the anode.

Appellants stated in the last paragraph on page 13 of the specification, line 19, that, when a reverse voltage is applied between the first terminal zone 30 and the second terminal zone 40, for which purpose the second terminal zone 40 is put at the potential of the substrate 10, for example, and the first terminal zone 30 is put at a positive potential, approximately the entire voltage is dropped across the drift zone 32, which is doped more lightly than the first and second terminal zones 30, 40.

Appellants explained on page 14 of the specification, line 1, that, in the semiconductor substrate 10, a space charge zone RLZ is formed proceeding from the first terminal zone 30. The

boundary of the space charge zone is shown using a dashed line in Fig. 1. The potential in the space charge zone RLZ continuously decreases proceeding from the first terminal zone 30 toward the boundaries of the space charge zone RLZ. In this case, the space charge zone RLZ extends over the length of the drift zone 32 below the insulation layer 20. In a similar way in which the potential in the drift zone 32 decreases proceeding from the first terminal zone 30 up to the second terminal zone 40 and reaches a minimum value there, the potential of the space charge zone RLZ in the substrate 10 below the insulation layer 20 also decreases proceeding from the first terminal zone 30. Because of the space charge zone RLZ that forms below the drift zone 32 in the substrate 10, the maximum voltage present at the insulation layer 20 between the drift zone 32 and the substrate 10 is lower than the maximum voltage that occurs. The maximum voltage that occurs corresponds to the difference between the potential at the first terminal zone 30 and the lowest potential GND to which the substrate 10 is connected.

As set forth in the last paragraph on page 14 of the specification, line 23, the voltage present at the insulation layer 20 is zero if the potential profile in the drift zone 32 corresponds to the potential profile in the space charge zone RLZ below the insulation layer 20. In the semiconductor

component, by virtue of the space charge zone RLZ which can form through the first terminal zone 30 bearing directly on the substrate 10, the insulation layer 20 is thus exposed to a lower voltage loading than would be the case in comparable components in which the first terminal zone does not adjoin the substrate. As a result, in the case of the inventive component, it is possible to use a thinner insulation layer 20 than in comparable components with the same dielectric strength, which in turn leads to a lower thermal resistance between the semiconductor layer 12 above the insulation layer 20 and the substrate 10. This results in better heat dissipation from the semiconductor layer 12 into the substrate 10 and to a heat sink connected, if appropriate, to the substrate 10.

Appellants outlined on page 15 of the specification, line 15, that Fig. 2 shows an exemplary embodiment of an inventive semiconductor component that is designed as an n-channel MOS transistor. The component has a semiconductor substrate 10 with an insulation layer 20 that is applied on the substrate 10, and a semiconductor layer 12 that is applied on the insulation layer. An n-doped first terminal zone 30, an n-doped second terminal zone 42, and a drift zone 32 located between the first and second terminal zones 30, 42 are formed in the semiconductor layer 12. The first terminal zone 30 is

doped complementary with respect to the substrate 10 and reaches through the insulation layer 20 right into the semiconductor substrate 10.

As set forth on page 16 of the specification, line 2, the drift zone 32 directly adjoins the first terminal zone 30. A p-doped depletion zone 50 is formed between the second terminal zone 42 and the drift zone 32. In the exemplary embodiment shown in Fig. 2, the first terminal zone 30 forms the drain zone, the second terminal zone 42 forms the source zone, and the depletion zone 50 forms the body zone (the body region) of the MOS transistor. A gate electrode 60 is applied above the depletion zone 50 and is insulated from the semiconductor layer 12 by an insulation layer 62.

Appellants also outlined on page 16 of the specification, line 12, that, when a potential that is positive relative to the reference-ground potential GND of the substrate 10 is applied to the drain zone 30 and when a lower potential, preferably the reference-ground potential GND, is applied to the source zone 42, a voltage drop occurs in the drift zone 32 between the drain zone 30 and the depletion zone 50 and a space charge zone RLZ is formed in the semiconductor substrate 10 proceeding from the drain zone 30, in which case the space charge zone RLZ can extend in the substrate 10 as far as below

the depletion zone 50. The maximum voltage drop between the drain zone 30 and the source zone 42 is achieved when the transistor is in the off state, that is to say when there is no suitable drive voltage present between the gate 60 and the source 42. The insulation layer 20 must be dimensioned for this case.

Appellants stated on page 17 of the specification, line 2, that, by virtue of the formation of the space charge zone RLZ, the maximum voltage present at the insulation layer 20 is smaller than the difference between the potential at the drain zone 30 and the reference-ground potential GND. The MOS transistor according to the invention can thus be operated with voltages which are higher than those for which the insulation layer 20 is designed. The MOS transistor according to the invention can therefore be realized together with MOS transistors for drive logic circuitry on the same insulation layer, in which case the insulation layer need only be designed for the lower voltages occurring in the drive logic circuitry.

Appellants also stated on page 17 of the specification, line 14, that the MOS transistor can be realized, for example, with a dielectric strength of up to 40 V on an insulation layer that has a thickness - designed for realizing drive logic

circuitry- of between 50 nm and 200 nm and is thus considerably thinner than the insulation layer normally designed for a dielectric strength of 40 V.

It is outlined in the last paragraph on page 17 of the specification, line 21, that, as shown in Fig. 2, the semiconductor layer 12 beside the transistor is preferably removed down to the insulation layer to insulate the transistor from other components (not illustrated) that are on the insulation layer 20. The connection between the transistor and the other components is effected in a wiring plane (not specifically illustrated) above the semiconductor layer 12.

Appellants stated on page 18 of the specification, line 4, that Fig. 3 shows an exemplary embodiment of a semiconductor component that is designed as a MOS transistor and that differs from that illustrated in Fig. 2 by virtue of the fact that the n-doped source zone 42 also extends through the insulation layer 20 right into the p-doped semiconductor substrate 10. This MOS transistor is suitable, in particular, as a so-called high-side switch, in which both the source terminal and the drain terminal can be at a high potential. If a potential which is positive relative to the reference-ground potential GND is present at the source zone 42, and if the drain zone 30 is at reference-ground potential, then the space

charge zone propagates in the semiconductor substrate 10 proceeding from the source zone 42.

Appellants further stated on page 18 of the specification, line 18, that, in the case where a potential that is positive relative to the reference-ground potential GND is present both at the drain zone 30 and at the source zone 42, a space charge zone propagates proceeding from the drain zone 30 and the source zone 42.

It is stated in the last paragraph on page 18 of the specification, line 24, that the transistor according to Fig. 3 furthermore differs from that illustrated in Fig. 2 by virtue of the fact that the transistor is formed symmetrically with regard to the source zone 42. Thus, in the example, the source zone 42 is adjoined on the left by a further depletion zone 52 with an overlying gate electrode 64, a drift zone 34 and a further drain zone (not illustrated). The two gate electrodes 60, 64 are connected to one another, and the two drain zones are connected to one another.

Appellants explained on page 19 of the specification, line 8, that the drift zone 32 may be of the same conduction type as the first terminal zone 30, i.e. the cathode in Fig. 1 and the drain zone D in Fig. 2, although the drift zone is doped more

weakly than the first terminal zone 30. One embodiment of the invention provides for the drift zone to have respectively complementary doped sections 32A-32F, as is illustrated in the case of the perspectively illustrated MOS transistor in Fig. 3. In the exemplary embodiment shown in Fig. 3, n-doped sections 32A, 32C, 32E and p-doped sections 32B, 32D, 32F alternate. The sections 32A-32F extend in the longitudinal direction between the depletion zone 50 and the drain zone 30. The n-doped sections 32A, 32C, 32E are connected to the n-doped drain zone 30 and the p-doped sections are connected to the p-doped depletion zone 50.

As set forth in the last paragraph on page 19 of the specification, line 23, the arrangement of complementary doped sections in the drift zone 32 is known from so-called compensation components. In this case, the n-doped sections 32A, 32C, 32E can be doped more highly than in the case of conventional components in which no complementary (p-doped) sections are present. The higher doping of the n-type sections 32A, 32C, 32E leads to a drift zone with a lower resistance when the component is in the on state, i.e. when a forward voltage is applied. When a reverse voltage is applied, the n-doped sections 32A, 32C, 32E and the p-doped sections 32B, 32D, 32F are mutually depleted, resulting in a high breakdown voltage.

Appellants stated on page 20 of the specification, line 9, that Fig. 4 shows a semiconductor component that is designed as a bipolar transistor, with a p-doped semiconductor substrate 10, an insulation layer 20 applied on the substrate 10, and a semiconductor layer 12 located on the insulation layer 20. An n-doped first terminal zone 30, an n-doped second terminal zone 42, a drift zone 32, and a p-doped depletion zone 50 located between the drift zone 32 and the second terminal zone 42 are formed in the semiconductor layer 12. The first terminal zone 30 forms the collector K of the transistor and extends through the insulation layer 20 right into the semiconductor substrate 10. The second terminal zone 42 forms the emitter E, and depending on the purpose for which the transistor is used, can extend like the collector K down into the substrate 10. The depletion zone 50 forms the base of the transistor.

References Cited:

Patent Number	Inventor	Issue Date
6,097,063	Fujihira	August 1, 2000
6,121,661	Assaderaghi et al.	September 19, 2000
6,221,737 B1	Letavic et al.	April 24, 2001

Issues

1. Whether or not claims 1-2, 5-6, 8, 10-11, and 13 are obvious over Fujihira together with Letavic et al. and Assaderaghi et al. under 35 U.S.C. §103.

Grouping of Claims:

Claim 1 is independent. Claims 2, 5-6, 8, 10-11, and 13 depend on claim 1. The patentability of claims 2, 5-6, 8, 10-11, and 13 are not separately argued. Therefore, claims 2, 5-6, 8, 10-11, and 13 stand or fall with claim 1.

Arguments:

In the second paragraph on page 2 of the final Office action, claims 1-2, 5-6, 8, 10-11, and 13 have been rejected as being unpatentable over Fujihira together with Letavic et al. and Assaderaghi et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> an insulation layer on said semiconductor substrate, said insulating layer having a thickness of between 50 nm and 200 nm;

...

at least one of said first doped terminal zone and said second doped terminal zone directly adjoining said semiconductor substrate. (Emphasis added.)

Fujihira describes a SOI (silicon-on-insulator) component with source and drain zones 8, 9, which form the first and second terminal zones in the sense of the invention of the instant application, and with a drift zone 1. These semiconductor zones are disposed above an insulation layer 6, which is disposed on a semiconductor substrate 5 (see Figs. 6A-6C). Therefore, Fujihira does not disclose "at least one of said first doped terminal zone and said second doped terminal zone directly adjoining said semiconductor substrate" as recited in claim 1 of the instant application.

Fujihira also does not disclose "said insulating layer having a thickness of between 50 nm and 200 nm" as recited in claim 1 of the instant application. The SOI component as shown in Figs. 6A-6C of Fujihira should have a breakdown voltage of 100 V (see column 12, line 4). Fujihira does not disclose how thick the insulation layer 6 should be in order to reach such a breakdown voltage. However, a person skilled in the art would know that the thickness of the insulation layer in the SOI component of Fujihira must be clearly more than 200 nm in order to reach a breakdown voltage of 100 V.

A publication Schwalke et al ("Ultra-Thick Gate Oxides: Charge Generation and Its Impact on Reliability," presented at the 10^{th} WODIM, Munich, November 13-15, 2000) is enclosed herewith for the edification of the Board and the Examiner. The chart on page 12 of this document shows the critical electric field strength of the semiconductor oxide layer depending on its thickness. The curve shows the critical electric field strength only up to an oxide thickness of 140 nm. However, this curve, which is approximately linear in this area, can be simply interpolated up to an oxide thickness of up to 200 nm. A critical electric field strength E_{crit} = 6 MV/cm at an oxide thickness of 200 nm can then be obtained. This means that an oxide layer with a thickness d = 200 nm will be destroyed by an electric field with a field strength E_{crit} = 6 MV/cm. This kind of field strength E_{crit} = 6 MV/cm corresponds to a voltage of $U_{crit} = E_{crit}.d$ = 120 V. Since electronic components must be constructed to avoid the occurrence of the critical operating condition during normal operation, safety factors should be considered. Even with a safety factor of 1.5, namely a maximum permitted field strength of 4 MV/cm, the oxide thickness for a breakdown voltage of 110 V is already required to be more than 250 nm ($d = U_{crit}/E_{crit}$ = 100 V/4 MV/cm).

In summary, although Fujihira does not disclose the thickness of the insulation layer 6, it is well known to a person skilled in the art that a breakdown voltage of 100 V requires the thickness of the insulation layer to be more than 250 nm.

Even if a person skilled in the art, with the knowledge of Assaderaghi et al., would provide for a conductive connection between the substrate 5 and the drain zone 9 or the source zone 8 in the component of Fujihira, he or she would have no reason to also reduce the thickness of the insulation layer to a value of between 50 nm and 200 nm. None of the cited references discloses that such an electrically conductive connection between one of the terminal zones and the substrate is suitable to reduce the voltage rating of the insulation layer by application of a voltage between the terminal zones as opposed to conventional components, so that the insulation layer can be thinner than those of the conventional power components which do not have such a conductive connection between one of the terminal zones and the substrate.

The thickness of 100 nm to 500 nm disclosed by Assaderaghi et al. and the thickness of 100 nm to 5000 nm disclosed by Letavic et al. do not provide enough of a hint to in fact reduce the thickness of the insulation layer to a value of below 200 nm because, taking into consideration the above

detailed explanation and according to the state of knowledge at that time, a person skilled in the art must have come to the conclusion that a thin oxide thickness is not enough to reach the desired breakdown voltage in Fujihira.

The Examiner has stated in the paragraph bridging pages 6 and 7 of the final Office action that 100 V disclosed by Fujihira is merely an "ideal" breakdown voltage and thus the breakdown voltage is not limited to 100 V. However, nothing in Fujihira suggests that the breakdown voltage be less than 100 V. What is not disclosed in the prior art reference cannot be read into the disclosure simply because it is possible. Rather, a hint or suggestion is required from the prior art.

In conclusion, it is not obvious for a person skilled in the art, starting from Fujihira, to choose an oxide thickness of between 50 nm and 200 nm and to provide a connection between at least one of the terminal zones and the substrate in order to arrive to the component according to claim 1 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since

all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Appellants

YC/bb

Date: September 24, 2004
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Florida 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Appendix - Appealed Claims:

1. A semiconductor component, comprising:

a semiconductor substrate;

an insulation layer on said semiconductor substrate, said insulating layer having a thickness of between 50 nm and 200 nm;

a semiconductor layer configured on said insulation layer;

a first doped terminal zone and a second doped terminal zone formed in said semiconductor layer; and

a drift zone formed in said semiconductor layer;

said drift zone formed between said first doped terminal zone and said second doped terminal zone, said drift zone including a plurality of complementary doped adjacent sections; and

at least one of said first doped terminal zone and said second doped terminal zone directly adjoining said semiconductor substrate.

2. The semiconductor component according to claim 1, wherein said first terminal zone and said second terminal zone reach through said insulation layer into said substrate.

5. The semiconductor component according to claim 1, comprising:

a depletion zone configured between said second terminal zone and said drift zone;

said depletion zone having a conduction type; and

said first terminal zone and said second terminal zone having a conduction type that is complementary to said conduction type of said depletion zone.

6. The semiconductor component according to claim 1, wherein:

said first terminal zone has a conduction type; and

said drift zone has a conduction type that is equivalent to the conduction type of said first terminal zone.

8. The semiconductor component according to claim 5, wherein:

said plurality of said complementary doped adjacent sections includes first sections and second sections;

said first sections and said first terminal zone are of a first conduction type;

said first sections are connected to said first terminal zone;

said second sections and said depletion zone are of a second conduction type complementary to said first conduction type; and

said second sections are connected to said depletion zone.

10. The semiconductor component according to claim 1, wherein said plurality of said complementary doped adjacent sections run in a longitudinal direction between said first terminal zone and said second terminal zone.

11. The semiconductor component according to claim 13, wherein:

said plurality of said complementary doped adjacent sections includes first sections and second sections;

said first sections and said first terminal zone are of a first conduction type;

said first sections are connected to said first terminal zone;

said second sections and said depletion zone are of a second conduction type complementary to said first conduction type; and

said second sections are connected to said depletion zone.

13. The semiconductor component according to claim 10, comprising:

a depletion zone configured between said second terminal zone and said drift zone;

said plurality of said complementary doped adjacent sections running between said first terminal zone and said depletion zone.

Ultra-Thick Gate Oxides: Charge Generation and Its Impact on Reliability

Udo Schwalke, Martin Pölzl, Thomas Sekinger,
Martin Kerber

Infineon Technologies AG, 81730 Munich, Germany

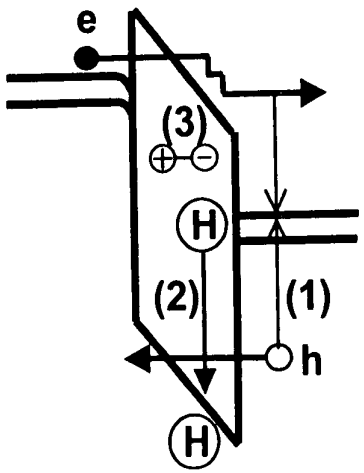
Vorgestellt bei der 10th WODIM, Munich 13.-15. Nov. 2000
p. 38

as appendix to Response of April 12, 2004

Outline

- **Introduction & Motivation**
- **Electrical Results**
  - I-V characteristics of ultra-thick gate oxides
  - Charge generation & trapping
  - Current transients: Effect of temperature & thickness
- **Discussion on Mechanism**
- **Interpretation of TDDB**
  - Weibull slope & voltage acceleration factor
- **Conclusion**

Introduction: Established TDDB Models



Tox: 5-25nm

1/E Model

(1) Anode hole injection model

(2) Hydrogen release model

$$t_{use} = C \cdot \left| \frac{t_{str}}{C} \right|^{E_{str}/E_{use}}$$

Linear E-Model

(3) Dipole related thermo-chemical model

$$t_{use} = t_{stress} \cdot \exp\left[\gamma \cdot \left(|E_{stress}| - |E_{use}|\right)\right]$$

Motivation

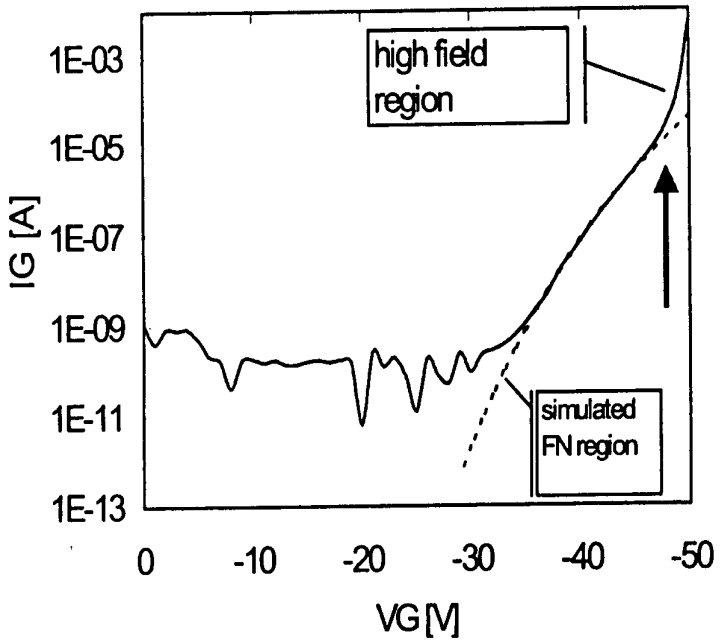
- MOS-based high-voltage power devices & HV-ICs rely on ultra-thick gate oxides (UTGOX); Tox: 50-150nm
- Stringent reliability requirements for power-MOS applications accurate lifetime predictions required
- However, present understanding of TDDB mechanisms in UTGOX not satisfying
- Established thin gate oxide (5-25nm) breakdown models (1/E or E) not appropriate for UTGOX:
  1. Abnormal voltage acceleration factors
  2. Weibull slope strongly depends on stress voltage

Lifetime predictions for UTGOX questionable

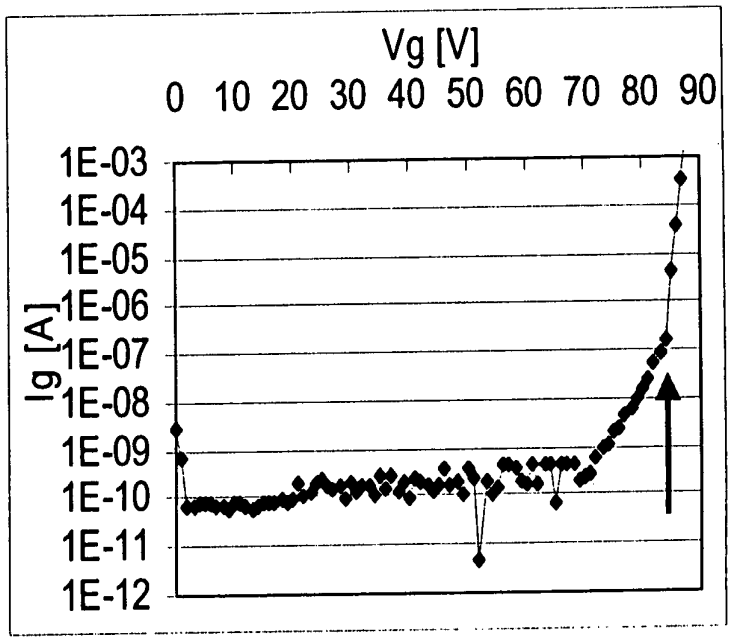
Study on breakdown mechanisms in UTGOX needed

Results: I-V Characteristics of UTGOX

Tox = 55 nm

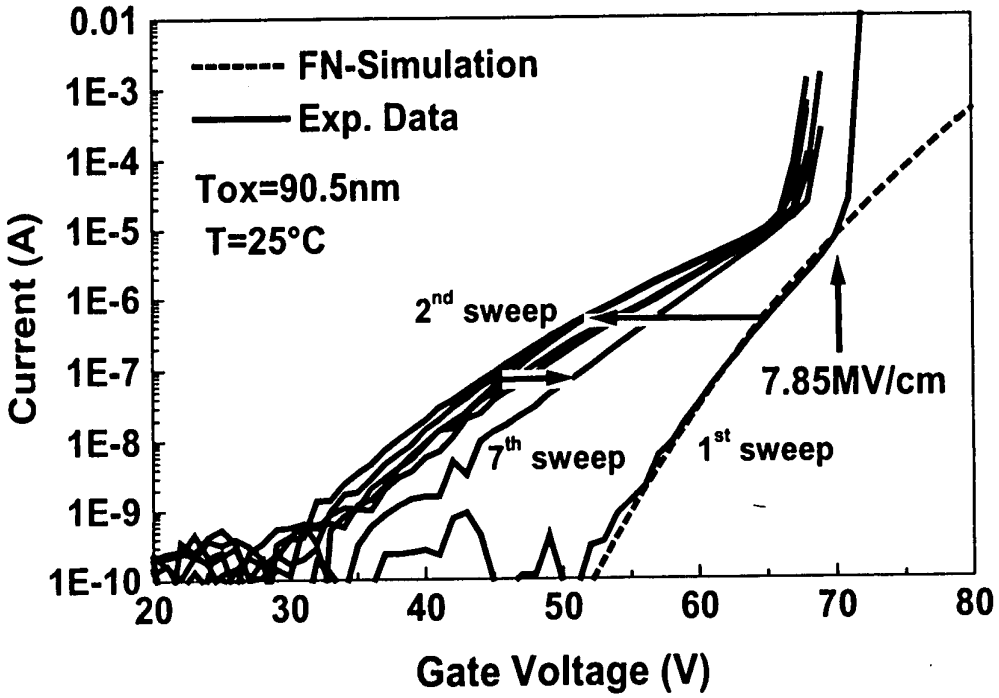


Tox = 120 nm



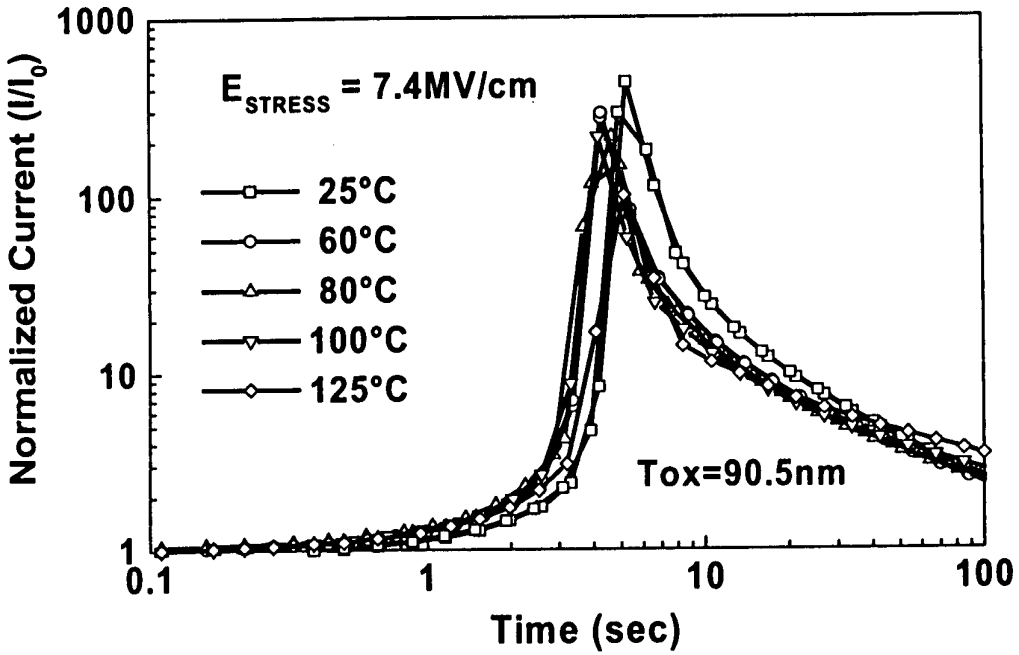
- UTGOX show enhanced conduction mode at higher fields. Dielectric breakdown?
- Independent of stress polarity

Charge Generation & Trapping



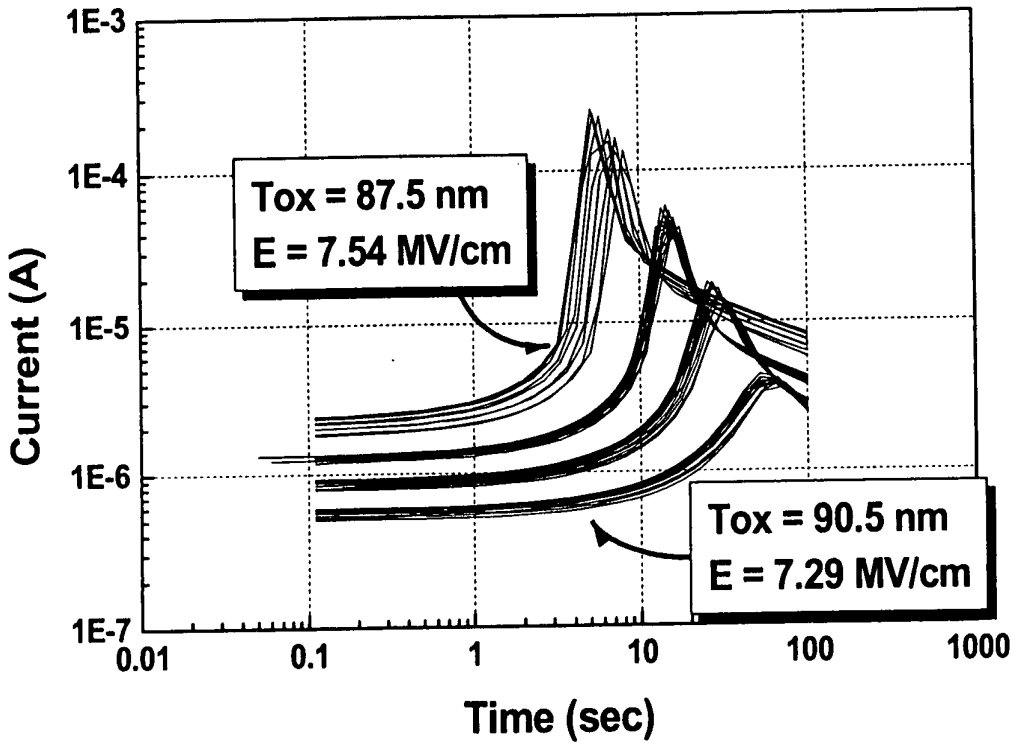
- Steep current increase: No breakdown
- Reversible mechanism & severe charge trapping
- What is the origin of the reversible high oxide conduction?

Current Transients: Effect of Temperature



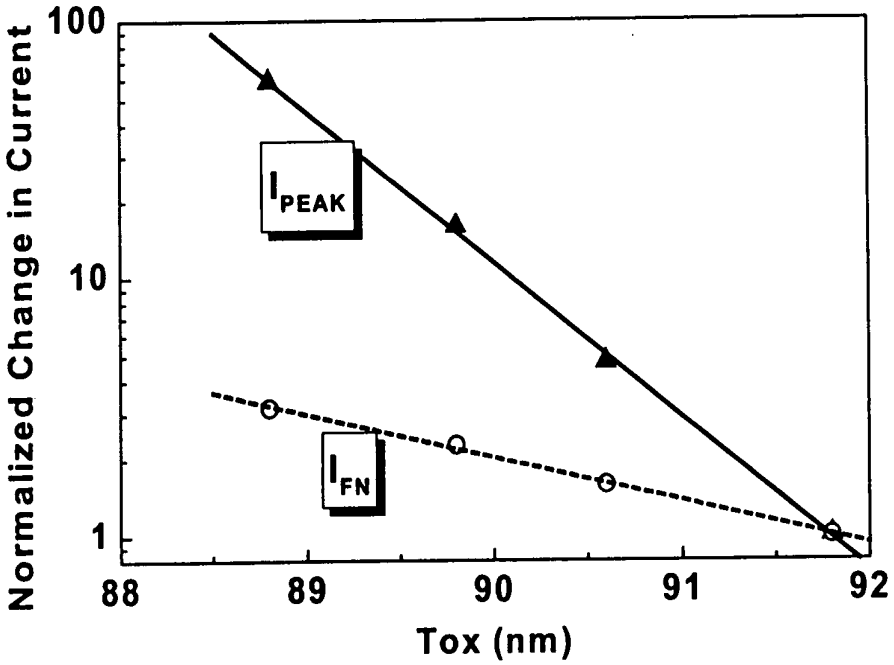
- Current transients not thermally activated
  not thermally activated ohmic conduction
  not related to Poole-Frenkel type mechanism

Current Transients: Effect of Thickness



- Strong dependence on oxide thickness variations & small changes in electric field

Current Transients: Correlation with FN



- Excessive charge generation not due to FN

Discussion on Mechanism

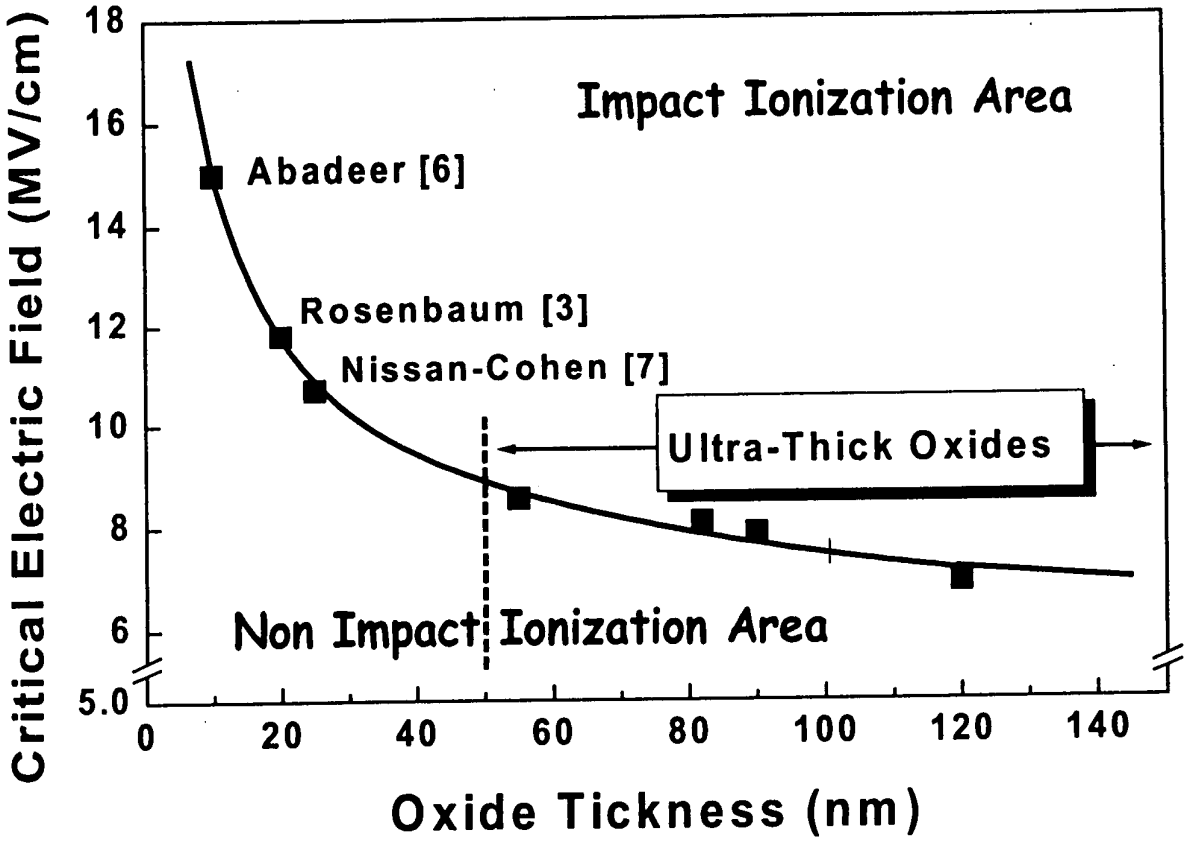
- Electrical results suggest very efficient charge generation mechanism in UTGOX other than via Fowler-Nordheim
- No evidence for thermally activated process
- However, extreme sensitivity on electric field & oxide thickness variation

Suggested mechanism for UTGOX:

Impact ionization (II) + electron-hole pair generation

Critical Field for Impact Ionization

- ⇒ Kritisches Feld für 200nm ≈ 6 MV/cm !
⇒ bei dieser Feldstärke beginnt die Zerstörung des Oxids
für kleine Durchbruchsfelder im Betrieb werden ca. 3 MV/cm angelegt !
⇒ d.h. für 100V sind Oxiddicken d_{ox} > 300nm erforderlich



- Critical field for II depends on Tox
- UTGOX: II dominates already at low E (≈ 8MV/cm)

Acknowledgments

Management:

Dr. Preussger, M. Obry (RM)

Dr. Werner, Dr. Kanert (AI QM)

Colleagues & Staff from RM:

T. Pompl, G. Diestl, W. Nissl, G. Innertsberger, K.H. Allers
E. Lepuschitz, R. Murr